CLAIMS:

1. A load line regulated switched mode power converter for supplying an output voltage (Vo) and an output current (Io) to a load (Zo), the switched mode power converter comprising:

an inductor (L), a switch (SW2) coupled to the inductor (L), a first impedance (Z1, Rs, Rcu), a second impedance (Z2, Rs), and

a power converter controller (10) comprising:

a first sense circuit (100) for obtaining momentary information (SI) on a first current (I1) flowing through the first impedance (Z1), the first current (I1) being related to the output current (Io),

means for determining (101) a difference between a zero load voltage (VID) and the output voltage (Vo) to obtain a difference signal (FD),

a second sense circuit (102) for obtaining further information (FI) on a second current (I2) flowing through the second impedance (Z2, Rs), the second current (I2) being related to the first current (I1),

an integrator (103) for integrating a difference between the further information (FI) and the difference signal (FD) to obtain a correction signal (CS), and

a switch controller (104, 105) for receiving the difference signal (FD), the momentary information (SI) and the correction signal (CS) to control the switch (SW2) for obtaining a substantially zero correction signal (CS) in a steady state.

2. A switched mode power converter as claimed in claim 1, wherein the momentary information (SI) has a bandwidth for instantaneously regulating the power converter, and wherein the further information (FI) has a further bandwidth lower than the first mentioned bandwidth.

3. A switched mode power converter as claimed in claim 1, wherein the switch controller (104, 105) comprises:

a driver (104) for receiving a first driver signal and a second driver signal to operate the switch (SW) when a level of the first driver signal reaches a level of the second driver signal, and

a means for receiving (105) the correction signal (CS) for correcting either:

(i) the momentary information (SI) to obtain corrected momentary information (CSI), wherein the first driver signal is the corrected momentary information (CSI) and the second driver signal is the difference signal (FD), or

(ii) the difference signal (FD) to obtain a corrected difference signal (CFD), wherein the first driver signal is the momentary information (SI) and the second driver signal is the corrected difference signal (CFD), or

(iii) the momentary information (SI) to obtain corrected momentary information (CSI) and the difference signal (FD) to obtain a corrected difference signal (CFD), wherein the first driver signal is the corrected momentary information (CSI) and the second driver signal is the corrected difference signal (CFD).

4. A switched mode power converter as claimed in claim 3, wherein the means for receiving (105) the correction signal (CS) comprises a multiplier receiving the difference signal (FD) and the correction signal (CS) to supply a multiplied difference signal as the corrected difference signal (CFD).

5. A switched mode power converter as claimed in claim 3, wherein the means for receiving (105) the correction signal (CS) comprises a multiplier receiving the momentary information (SI) and the correction signal (CS) to supply multiplied momentary information as the corrected momentary information (CSI).

6. A switched mode power converter as claimed in claim 3, wherein the means for receiving (105) the correction signal (CS) comprises means for introducing an offset receiving the difference signal (FD) and the correction signal (CS) to supply the corrected difference signal (CFD) having an offset.

7. A switched mode power converter as claimed in claim 3, wherein the means for receiving (105) the correction signal (CS) comprises means for introducing an offset receiving the momentary information (SI) and the correction signal (CS) to supply the corrected momentary information (CSI) having an offset.

8. A switched mode power converter as claimed in claim 4 or 5, wherein the power converter controller (10) comprises a load determining circuit (SCC; 1032) for supplying a load signal (SWS1; SWS2) indicating whether a load condition of said power converter is above a first predetermined load condition (LI3), and a window circuit (SE2; SE1) for controlling the integrator (103) to determine the correction signal (CS1) only during a period in time the load signal (SWS1; SWS2) indicates that the load condition is above the first predetermined load condition (LI3) to obtain predominantly a correction of a slope of the load line.

9. A switched mode power converter as claimed in claim 6 or 7, wherein the power converter controller (10) comprises a load determining circuit (SCC; 1032) for supplying a load signal (SWS1; SWS2) indicating whether a load condition of said power converter is below a second predetermined load condition (LI2), and a window circuit (SE2; SE1) for controlling the integrator (103) to determine the correction signal (CS2) only during a period in time the load signal (SWS1; SWS2) indicates that the load condition is below the second predetermined load condition (LI2) to obtain predominantly a DC-shift of the load line.

10. A switched mode power converter as claimed in claim 3, wherein:

the means for receiving (105) the correction signal (CS) comprises a multiplier (M1, M2) receiving:

(i) the difference signal (FD) and a first correction signal (CS1) to supply the corrected difference signal (CFD) being a multiplied difference signal (FD), or

(ii) the momentary information (SI) and the first correction signal (CS1) to supply the corrected momentary information (CSI) being multiplied momentary information (SI),

the means for receiving (105) the correction signal (CS) further comprises means for introducing an offset (OM1, OM2) receiving:

(i) the difference signal (FD) and a second correction signal (CS2) to supply the corrected difference signal (CFD) being the difference signal (FD) having an offset, or

(ii) the momentary information (SI) and the second correction signal (CS2) to supply the corrected momentary information (CSI) being the momentary information (SI) having an offset,

the power converter controller (10) comprises a load determining circuit (SCC; 1032) for supplying a load signal (SWS1; SWS2) indicating whether a load condition of said power converter is above a first predetermined load condition (LI3) or below a second predetermined load condition (LI2), and a window circuit (SE2; SE1) for controlling the integrator (103) to determine the first correction signal (CS1) only during a period in time the load signal (SWS1; SWS2) indicates that the load condition is above the first predetermined load condition (LI3), and to determine the second correction signal (CS2) only during a period in time the load signal (SWS1; SWS2) indicates that the load condition is below the second predetermined load condition (LI2), and wherein the first predetermined load condition (LI3) is higher than the second predetermined load condition (LI2).

11. A switched mode power converter as claimed in claim 9, wherein said power converter comprises storage means (1030, 1031) for storing the first correction signal (CS1) and the second correction signal (CS2).

12. A switched mode power converter as claimed in claim 8, 9 or 10, wherein the load condition is determined by the level of the output voltage Vo, or by the level of the difference signal (FD), or by the output current (Io), or by a current related to the output current (Io).

13. A switched mode power converter as claimed in claim 1, wherein the first impedance (Z1) and the second impedance (Z2) are the same common resistor (Rs), and wherein the first current (I1) and the second current (I2) are the same current (Is).

14. A switched mode power converter as claimed in claim 1, wherein the first impedance (Z1) is an impedance of the main current path of the switch (SW2).

15. A switched mode power converter as claimed in claim 1, wherein the first impedance (Rcu) is arranged in series with the inductor (L).

16. A switched mode power converter as claimed in claim 1, wherein the second impedance (Rs) is arranged between an input of the power converter and a main current path of the switch (SW2) for sensing an average input current (Is) of the power converter.

17. A switched mode power converter as claimed in claim 13, wherein the power converter is a down-converter comprising a series arrangement of main current paths of the first mentioned switch (SW2) and a further switch (SW1), the inductor (L) being arranged between a junction of the main current paths and an output of the power converter, and wherein the common resistor (Rs) is arranged in series with the main current path of the first mentioned switch (SW2).

18. A switched mode power converter as claimed in claim 1, wherein the means (101) for determining the difference comprises a third resistor (R1) arranged between a reference voltage (VID) and the output voltage (Vo) to obtain a difference voltage across the third resistor (R1), the difference signal (FD) being related to the difference voltage.

19. A switched mode power converter as claimed in claim 18, wherein

the means (101) for determining the difference is arranged to supply a difference current (FD) being related to the voltage across, or a current through the third resistor (R1),

the second sense circuit (102) is arranged for supplying an information current (FI) being related to the voltage across (Vs) or the current through (Is) the common resistor (Rs), and

the integrator comprises a capacitor 103 for integrating the difference current (FD) and the information current (FI) to obtain the correction signal (CS).

20. A switched mode power converter as claimed in claim 1, wherein

the power converter is a down-converter comprising a series arrangement of main current paths of the first mentioned switch (SW2) and a further switch (SW1), the inductor (L) being arranged between a junction of the main current paths and an output of the power converter,

a smoothing capacitor (Ce) is coupled to a terminal of the main current path of the first mentioned switch (SW2) directed towards the input of the power converter, and

the second impedance (Rs) is arranged between the input of the power converter and the main current path of the first mentioned switch (SW2).

21. A switched mode power converter as claimed in claim 20, wherein the means (101) for determining the difference comprises a third resistor (R1) arranged between a

reference voltage (VID) and the output voltage (Vo) to obtain a difference voltage across the third resistor (R1), the difference signal (FD) being related to the difference voltage.

22. A switched mode power converter as claimed in claim 21, wherein:

the means (101) for determining the difference is arranged to supply a difference current (FD) being related to the voltage across, or a current through the third resistor (R1),

the second sense circuit (102) is arranged for supplying an information current (FI) being related to the voltage across (Vs) or the current through (Is) the second impedance (Rs), and

the integrator (103) comprises a capacitor (103) for integrating the difference current (FD) and the information current (FI) to obtain the correction signal (CS).

23. A load line regulated multiphase switched mode power converter comprising:

a first switched mode power converter (SMPSa) and a second switched mode power converter (SMPSb) being arranged in parallel to supply a total output current (Io) to a load (Co, Ro),

a power converter controller (10), a first impedance (Rs), and

a first sense circuit (102) for obtaining first information (FI) on a first current (Is) flowing through the first impedance (Rs), the first current (Is) being related to the total output current (Io),

means (101) for determining a difference between a zero load voltage (VID) and an output voltage (Vo) of the multiphase switched mode power converter to obtain a difference level (FD),

means (103) for integrating a difference between the first information (FI) and the difference level (FD) to obtain a correction signal (CS), and wherein

the first switched mode power converter (SMPSa) comprises:

a first inductor (L1a), a first switch (SW2a) coupled to the first inductor (L1a), a second impedance (Rds-ona), and wherein

the power converter controller (10) further comprises:

a second sense circuit (100a) for obtaining second information (SIa) on a second current (ISW2a) flowing through the second impedance (Rds-ona), the second current (ISW2a) being related to an output current (Ioa) of the first switched mode power converter (SMPSa), the second information (SIa) being momentary information,

first means (105a) for receiving the correction signal (CS), the difference level (FD) and the second information (SIa) to correct an amplitude of either the second information (SIa) or the difference level (FD), or both, to control a switch-off instant of the first switch (SW2a) to decrease a value or level of the correction signal (CS),

the second switched mode power converter (SMPSb) comprises:

a second inductor (L1b), a second switch (SW2b) coupled to the second inductor (L1b), a third impedance (Rds-onb), and wherein

the power converter controller (10) further comprises:

a third sense circuit (100b) for obtaining third information (SIb) on a third current (ISW2b) flowing through the third impedance (Rds-onb), the third current (ISW2b) being related to an output current (Iob) of the second switched mode power converter (SMPSb), the third information (SIb) being momentary information,

second means (105b) for receiving the correction signal (CS), the difference level (FD) and the third information (SIb) to correct an amplitude of either the third information (SIb) or the difference level (FD), or both, to control a switch-off instant of the second switch (SW2b) to decrease a value or level of the correction signal (CS).

24. An electronics apparatus comprising the switched mode power converter of claim 1, or the multiphase switched mode power converter of claim 23.

25. An electronics apparatus as claimed in claim 24, comprising a personal computer (PC), the output current (Io) of the switched mode power converter of claim 1, or the output current (Io) of the multiphase switched mode power converter of claim 16 being supplied to a processor (UP) of the personal computer (PC).

26. A power converter controller (10) for controlling a load line regulated power converter having a switch (SW2), the power converter controller (10) comprising:

a first sense circuit (100) for obtaining momentary information (SI) on a first current (I1) flowing in the power converter, the first current (I1) being related to an output current (Io) of the power converter,

means for determining (101) a difference between a zero load voltage (VID) and an output voltage (Vo) of the power converter to obtain a difference signal (FD),

a second sense circuit (102) for obtaining further information (FI) on a second current (I2) flowing in the power converter, the second current (I2) being related to the first current (I1),

an integrator (103) for integrating a difference between the further information (FI) and the difference signal (FD) to obtain a correction signal (CS), and

a switch controller (104, 105) for receiving the difference signal (FD), the momentary information (SI) and the correction signal (CS) to control the switch (SW2) for obtaining a substantially zero correction signal (CS) in a steady state.

27. A power converter controller (10) for controlling a multiphase switched mode power converter comprising a first switched mode power converter (SMPSa) and a second switched mode power converter (SMPSb) being arranged in parallel to supply a total output current (Io) to a load (Co, Ro),

the power converter controller (10) comprising:

a first sense circuit (102) for obtaining first information (FI) on a first current (Is) flowing in the multiphase switched mode power converter, the first current (Is) being related to the total output current (Io),

means (101) for determining a difference between a zero load voltage (VID) and an output voltage (Vo) of the multiphase switched mode power converter to obtain a difference level (FD),

means (103) for integrating a difference between the first information (FI) and the difference level (FD) to obtain a correction signal (CS),

a second sense circuit (100a) for obtaining second information (SIa) on a second current (ISW2a) flowing in the first switched mode power converter (SMPSa), the second current (ISW2a) being related to an output current (Ioa) of the first switched mode power converter (SMPSa), the second information (SIa) being momentary information,

first means (105a) for receiving the correction signal (CS), the difference level (FD) and the second information (SIa) to correct an amplitude of either the second information (SIa) or the difference level (FD), or both, to control a switch-off instant of the first switch (SW2a) to decrease a value or level of the correction signal (CS),

a third sense circuit (100b) for obtaining third information (SIb) on a third current (ISW2b) flowing in the second switched mode power converter (SMPSb), the third current (ISW2b) being related to an output current (Iob) of the second switched mode power converter (SMPSb), the third information (SIb) being momentary information, and

second means (105b) for receiving the correction signal (CS), the difference level (FD) and the third information (SIb) to correct an amplitude of either the third information (SIb) or the difference level (FD), or both, to control a switch-off instant of the second switch (SW2b) to decrease a value or level of the correction signal (CS).